ABSTRACT OF THE DISCLOSURE

A bus bridge circuit is connected to first and second buses and performs data transfer between devices. In the bus bridge circuit, a new parity bit is generated from a parity bit generated by a first PCI device and from a byte enable signal from a second PCI device, and is transmitted to the second PCI device, together with read data from the first PCI device. Consequently even if the byte enable values are different on the primary-side and secondary-side buses, parity errors on the secondary-side bus can be correctly transmitted to the primary-side bus.